

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/536,037
Filing Date March 27, 2000
Inventor Weimin (Michael) Li
Assignee Micron Technology, Inc.
Group Art Unit 2822
Examiner Toniae M. Thomas
Attorney's Docket No. MI22-1398
Customer No. 021567
Title: Low k Interlevel Dielectric Layer Fabrication Methods



To: Box RCE
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

From: James E. Lake
(Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828
509-624-4276

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

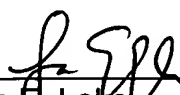
References -- See Attached Form PTO-1449

This Request for Continued Examination (RCE) Application is being filed in an abundance of caution to ensure consideration of the references listed on the attached form PTO-1449.

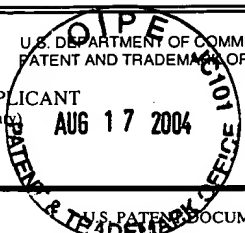
The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether the submitted references are prior art.

Respectfully submitted,

Dated: 17 Aug 2004

By: 
James E. Lake
Reg. No. 44,854

EL979952141

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE 		ATTY. DOCKET NO. MI22-1398		SERIAL NO. 09/536,037	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Weimin Li, et al.			
				FILING DATE March 27, 2000		GROUP 2822	
U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	6,153,504	11/2000	Shields et al			
	AB	4,971,655	11/1990	Stafano et al			
	AC	6,498,084 B2	12,2002	Bergemont			
	AD	5,036,383	07/1991	Mori			
	AE	5,593,741	01/1997	Ikeda			
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
FOREIGN PATENT DOCUMENTS							
	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	AM	08-045926A	02/1996	Japan			
	AN	JP8051058	02/1996	Japan			
	AO	JP63316476	12/1998	Japan			
	AP	JP8078322	03/1996	Japan			
	AQ	10-163083	06/1998	Japan			
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR	Wolf, S., Silicon Processing for the VLSI ERA. Vol. 3, The Submicron MOSFET p. 635					
	AS						
	AT						
EXAMINER				DATE CONSIDERED			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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COPY

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

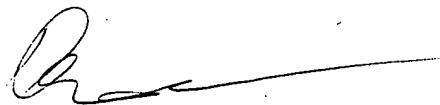
In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed after the filing of the Request for Continued Examination (RCE) Application and before receipt of the first Office Action. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. §1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional application of co-pending application Serial No. 09/388,826, filed September 1, 1999. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2). Citation of these references is respectfully requested.

Respectfully submitted,

Date: 2/11/04



David G. Latwesen Ph.D.
Reg. No. 38,533

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Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-1398		SERIAL NO. 09/536,037	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Weimin Li, et al.			
				FILING DATE March 27, 2000		GROUP 2822	

U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	6,503,818 B1	01/2003	Jang			
	AB	6,486,061 B1	11/2002	Xia et al.			
	AC	6,486,057 B1	11/2002	Yeh et al.			
	AD	6,465,372 B1	10/2002	Xia et al.			
	AE	6,444,593 B1	09/2002	Ngo et al.			
	AF	6,436,808 B1	08/2002	Ngo et al.			
	AG	6,435,943 B1	08/2002	Chang et al.			
	AH	6,429,115 B1	08/2002	Tsai et al.			
	AI	6,284,677 B1	09/2001	Hsiao et al.			
	AJ	6,030,901	02/2000	Hopper et al.			
	AK	6,133,618	10/2000	Steiner			
	AL	5,994,217	11/1999	Ng			

FOREIGN PATENT DOCUMENTS							
Document Number	Date	Country	Class	Subclass	Translation		
					Yes	No	
AM	8046186	02/1996	Japan				
AN	8046186	2/1996	Japan		X		
AO	7201716	08/1995	Japan				
AP	7201716	08/1995	Japan		X		
AQ	8046188	02/1996	Japan				

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)		
AR		Wolf, S., Silicon Process., V.1 407-413
AS		Wolf, S., Silicon Process., Vol. 2 48-49 and 435
AT		

EXAMINER	DATE CONSIDERED
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Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-1398		SERIAL NO. 097536,037	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Weimin Li, et al.			
				FILING DATE March 27, 2000		GROUP 2822	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,985,519	11/1999	Kakamu et al.			
	AB	5,747,388	05/1998	Kusters et al			
	AC	5,639,687	06/1997	Roman et al			
	AD	5,498,555	03/1996	Lin			
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FOREIGN PATENT DOCUMENTS							
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	AO						
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
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	AT						
EXAMINER				DATE CONSIDERED			
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FEB-12-2004 10:06	WELLS ST JOHN PS	5098383424 P.01
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE		
Patent Application Serial No. 09/536,037		
Filing Date March 27, 2000		
Inventor Weimin Li		
Assignee Micron Technology, Inc.		
Group Art Unit 2822		
Examiner T. Thomas		
Attorney Docket No. MI22-1398		
Title: Low k Interlevel Dielectric Layer Fabrication Methods		
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Commissioner for Patents P.O. Box 1450 Art Unit 2822 Alexandria, VA 22313-1450		
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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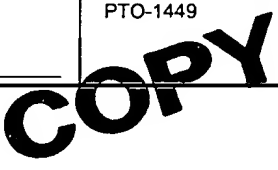
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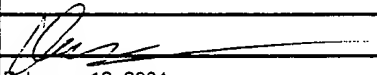
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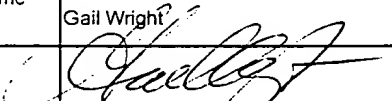
TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/536,037
	Filing Date	March 27, 2000
	First Named Inventor	Weimin Li
	Art Unit	2822
	Examiner Name	T. Thomas
Total Number of Pages in This Submission	Attorney Docket Number	MI22-1398

ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input checked="" type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation <input type="checkbox"/> Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____	<input type="checkbox"/> After Allowance communication to Technology Center (TC) <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): PTO-1449
Remarks <div style="text-align: center;">  </div>		
Customer No. 021567 The Commissioner is hereby authorized to charge any additional fees required under 37 C.F.R. Section 1.16 and Section 1.17 and credit any overpayments to account no. 23-0925.		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	David G. Latwesen Ph.D. Reg. No. 38,533; Wells St. John P.S.		
Signature			
Date	February 12, 2004		

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I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.			
Typed or printed name	Gail Wright		
Signature		Date	February 12, 2004

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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